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ICW

Practitioner's Docket No. 2550/111

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Wenhua Yang

Application No.: 09/932,216

Group No.: 2816

Filed: 08/17/2001

Examiner: Cunningham, T.

For: Bootstrap Module for Multi-Stage Circuit

**RESPONSE UNDER
37 C.F.R. § 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP
2816**

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT OR RESPONSE AFTER FINAL REJECTION--TRANSMITTAL

1. Transmitted herewith is an amendment after final rejection (37 C.F.R. 1.116) for this application.

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*

*(When using Express Mail, the Express Mail label number is mandatory;
Express Mail certification is optional.)*

I hereby certify that, on the date shown below, this correspondence is being:

MAILING

[X] deposited with the United States Postal Service in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

37 C.F.R. § 1.8(a)

[X] with sufficient postage as first class mail.

37 C.F.R. § 1.10*

☐ as "Express Mail Post Office to Addressee"

Mailing Label No. _____ (mandatory)

TRANSMISSION

☐ facsimile transmitted to the Patent and Trademark Office, (571) 273 - 8300.

Signature

Alexander J. Smolenski

(type or print name of person certifying)

* Only the date of filing (§ 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under § 1.8 continues to be taken into account in determining timeliness. See § 1.703(f). Consider "Express Mail Post Office to Addressee" (§ 1.10) or facsimile transmission (§ 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.

STATUS

2. Applicant is other than a small entity.

EXTENSION OF TERM

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

FEE FOR CLAIMS

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

	(Col.1)		(Col. 2)	(Col. 3)	OTHER THAN SMALL ENTITY			
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE	ADDIT. FEE	
TOTAL	22	MINUS	35	= 0	x	\$ 50.00	= \$	0.00
INDEP	4	MINUS	6	= 0	x	\$ 200.00	= \$	0.00
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+	\$ 0.00	= \$	0.00
TOTAL							\$	0.00
ADDIT. FEE								

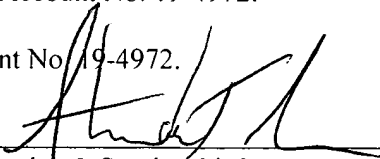
No additional fee for claims is required.

FEE DEFICIENCY

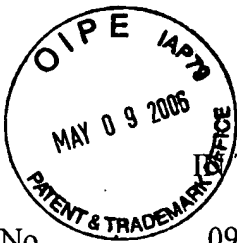
5. If any extension and/or fee is required, charge Account No. 19-4972.

If any fee for claims is required, charge Account No. 19-4972.

Date: May 5, 2006


Alexander J. Smolenski, Jr.
Registration No. 47,953
Bromberg & Sunstein LLP
125 Summer Street
Boston, MA 02110
U.S.
617-443-9292
Customer No. 02101

02550/00111 493911.1



THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 09/932,216
Applicant : Yang
Filed : August 17, 2001
TC/A.U. : 2816
Examiner : Terry D. Cunningham
Title: BOOTSTRAP MODULE FOR MULTI-STAGE CIRCUIT
Docket No. : 2550/111
Customer No. : 5542

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service in an envelope as first class mail with sufficient postage addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on May 5, 2005.

Alexander J. Smolenski, Jr.

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 C.F.R. §1.116-EXPEDITED PROCEDURE
EXAMINING GROUP 2816

Response F

Dear Sir:

In response to the final office action dated March 7, 2006, Applicants submit the following remarks:

Claims begin on page 2 of this paper, and

Remarks begin on page 7 of this paper.

An **Appendix** is attached following page 10 of this paper, including: page 55 of Weste, Neil and Eshraghian, Kamran, *Principles of CMOS VLSI Design*, Addison-Wesley, Reading, Massachusetts, 1985; and page 1-6 of Rung-Bin Lin, Chapter 1: Introduction to CMOS Circuits, http://vlsi.cse.yzu.edu.tw/education/vlsi_design/chapter1.pdf).